

### AMENDMENTS TO THE CLAIMS

Please amend Claims 6-7 and 25 as follows.

1. (Original) A process of fabricating a bottom electrode for a DRAM cell capacitor, comprising:
  - forming a container in an insulating layer overlying a semiconductor substrate, the insulating layer having a top surface;
  - lining the container with a hemispherical grained silicon layer;
  - depositing a metal nitride layer over the hemispherical grained silicon layer;
  - filling a remainder of the container with a photoresist;
  - removing the photoresist, the metal nitride layer and the hemispherical grained silicon layer down to the top surface; and
  - subsequently recessing the metal nitride layer and the hemispherical grained silicon layer by preferentially partially removing the metal nitride layer and the hemispherical grained silicon layer relative to the phototresist.
2. (Original) The process of Claim 1, wherein preferentially partially removing the metal nitride layer and the hemispherical grained silicon layer relative to the phototresist comprises selectively partially removing the metal nitride layer before selectively partially removing the hemispherical grained silicon layer.
3. (Original) The process of Claim 2, wherein selectively partially removing the metal nitride layer comprises exposing the metal nitride layer to a peroxide solution.
4. (Original) The process of Claim 3, wherein exposing the metal nitride layer to a peroxide solution comprises exposing the metal nitride layer to an ammonium peroxide mixture at a temperature between about 20°C and about 55°C.
5. (Original) The process of Claim 4, wherein the temperature is between about 30°C and about 40°C.
6. (Currently Amended) The process of Claim 4, wherein the ammonium peroxide mixture comprises between about 0.33 and about 4.8 weight percent H<sub>2</sub>O<sub>2</sub> and between about 0.18 and about 3.9 weight percent [[H<sub>2</sub>O<sub>2</sub>]]NH<sub>4</sub>OH.
7. (Currently Amended) The process of Claim 6, wherein the ammonium peroxide mixture comprises between about 0.70 and about 1.50 weight percent H<sub>2</sub>O<sub>2</sub> and between about 0.25 and about 0.75 weight percent [[H<sub>2</sub>O<sub>2</sub>]]NH<sub>4</sub>OH.

8. (Original) The process of Claim 3, wherein exposing the metal nitride layer to a peroxide solution comprises exposing the metal nitride layer to a hydrochloric acid peroxide mixture at a temperature between about 20°C and about 70°C.

9. (Original) The process of Claim 8, wherein the hydrochloric acid peroxide mixture comprises between about 0.33 and about 4.8 weight percent H<sub>2</sub>O<sub>2</sub> and between about 0.18 and about 4.9 weight percent HCl.

10. (Original) The process of Claim 9, wherein the hydrochloric acid peroxide mixture comprises between about 0.90 and about 1.60 weight percent H<sub>2</sub>O<sub>2</sub> and between about 0.50 and about 1.00 weight percent HCl.

11. (Original) The process of Claim 1, wherein the metal nitride comprises titanium nitride.

12. (Original) The process of Claim 1, wherein removing the photoresist, the metal nitride layer and the hemispherical grained silicon layer down to the top surface comprises subjecting the photoresist, the metal nitride layer and the hemispherical grained silicon layer to chemical mechanical polishing.

13. (Original) The process of Claim 1, wherein forming the container comprises forming a cylindrical open volume.

14. (Original) The process of Claim 1, wherein preferentially partially removing the metal nitride layer and the hemispherical grained silicon layer relative to the phototresist comprises etching the metal nitride layer, the hemispherical grained silicon layer and the phototresist, wherein the metal nitride layer and the hemispherical grained silicon layer are etched down farther below the top surface than the photoresist.

15. (Original) The process of Claim 14, wherein the metal nitride layer and the hemispherical grained silicon layer are etched at a rate ten times greater than the rate at which the photoresist is etched while preferentially partially removing the metal nitride layer and the hemispherical grained silicon.

16. (Original) The process of Claim 15, wherein the metal nitride layer and the hemispherical grained silicon layer are etched at a rate fifteen times greater than the rate at which the photoresist is etched while preferentially partially removing the metal nitride layer and the hemispherical grained silicon.

17-18. (Cancelled).

19. (Previously presented) A method of semiconductor fabrication, comprising:  
providing a surface on a substrate, the surface comprising metal nitride and a photoresist, wherein the metal nitride comprises titanium nitride; and  
selectively recessing the metal nitride relative to the photoresist, wherein selectively recessing comprises recessing the metal nitride layer down to a depth of between about 100 Å and about 500 Å below the surface.
20. (Original) The method of Claim 19, wherein the depth is between about 150 Å and about 250 Å below the surface.
21. (Original) The method of Claim 20, wherein the depth is about 200 Å below the surface.
22. (Previously presented) A method of semiconductor fabrication, comprising:  
providing a surface on a substrate, the surface comprising metal nitride and a photoresist, wherein the metal nitride comprises titanium nitride; and  
selectively recessing the metal nitride relative to the photoresist, wherein selectively recessing comprises etching the metal nitride layer at a temperature between about 20°C and about 70°C.
23. (Previously presented) The method of Claim 19, wherein selectively recessing comprises exposing the metal nitride to a peroxide mixture chosen from the group consisting of an ammonium hydroxide/peroxide mixture (APM) and a hydrochloric acid/peroxide mixture (HPM).
24. (Previously presented) The method of Claim 23, wherein the selectively recessing comprises employing an APM with between about 0.33 and about 4.8 weight percent H<sub>2</sub>O<sub>2</sub> and between about 0.18 and about 3.9 weight percent NH<sub>4</sub>OH.
25. (Currently Amended) The method of Claim 24, wherein the APM comprises between about 0.70 and about 1.50 weight percent H<sub>2</sub>O<sub>2</sub> and between about 0.25 and about 0.75 weight percent [[H<sub>2</sub>O<sub>2</sub>]]NH<sub>4</sub>OH.
26. (Original) The method of Claim 23, wherein selectively recessing comprises employing an HPM with between about 0.33 and about 4.8 weight percent H<sub>2</sub>O<sub>2</sub> and between about 0.18 and about 4.9 weight percent HCl.

27. (Original) The method of Claim 26, wherein the HPM comprises employing an HPM with between about 0.90 and about 1.60 weight percent  $H_2O_2$  and between about 0.50 and about 1.00 weight percent HCl.

28. (Previously presented) The method of Claim 19, wherein the surface further comprises an insulating layer and the metal nitride extends vertically along a vertical wall of the insulating layer.

29. (Original) The method of Claim 28, wherein the insulating layer comprises borophosphosilicate glass.

30. (Original) The method of Claim 28, wherein the surface further comprises a hemispherical grained silicon layer extending vertically adjacent to the metal nitride and further comprising selectively recessing a hemispherical grained silicon layer after selectively recessing the metal nitride, wherein the hemispherical grained silicon layer is directly adjacent the metal nitride layer.

31. (Original) The method of Claim 28, further comprising heating the substrate for about 30 to 120 seconds at between about  $130^{\circ}C$  and about  $250^{\circ}C$  before selectively recessing.

32. (Original) The method of Claim 31, wherein the substrate is heated to between about  $130^{\circ}C$  and about  $200^{\circ}C$  before selectively recessing.

33. (Cancelled).

34. (Previously presented) A method of fabricating an integrated circuit, comprising:  
providing a structural material on a semiconductor substrate, the structural material having a container;

depositing a metal nitride layer inside the container;

preferentially partially removing the metal nitride layer by exposing the metal nitride layer to a peroxide mixture,

wherein exposing the metal nitride layer to a peroxide mixture comprises maintaining the semiconductor substrate at a temperature between about  $20^{\circ}C$  and about  $55^{\circ}C$ , wherein the peroxide mixture is an ammonium hydroxide/peroxide mixture (APM) comprising between about 0.33 and about 4.8 weight percent  $H_2O_2$  and between about 0.18 and about 3.9 weight percent  $NH_4OH$ .

35. (Previously presented) The method of Claim 34, wherein the APM comprises between about 0.70 and about 1.50 weight percent  $\text{H}_2\text{O}_2$  and between about 0.25 and about 0.75 weight percent  $\text{NH}_4\text{OH}$ .

36. (Previously presented) A method of fabricating an integrated circuit, comprising:  
providing a structural material on a semiconductor substrate, the structural material having a container;

depositing a metal nitride layer inside the container;

preferentially partially removing the metal nitride layer by exposing the metal nitride layer to a peroxide mixture,

wherein exposing the metal nitride layer to a peroxide mixture comprises maintaining the semiconductor substrate at a temperature between about  $20^\circ\text{C}$  and about  $55^\circ\text{C}$ , wherein the peroxide mixture is a hydrochloric acid/peroxide mixture (HPM) comprising between about 0.33 and about 4.8 weight percent  $\text{H}_2\text{O}_2$  and between about 0.18 and about 4.9 weight percent  $\text{HCl}$ .

37. (Original) The method of Claim 36, wherein the HPM comprises between about 0.90 and 1.60 weight percent  $\text{H}_2\text{O}_2$  and between about 0.50 and about 1.00 weight percent  $\text{HCl}$ .

38. (Currently Amended) The method of Claim 34, wherein the temperature is between about  $30^\circ\text{C}$  and about  $40^\circ\text{C}$ .

39. (Previously presented) The method of Claim 34, wherein the metal nitride comprises titanium nitride.

40. (Original) A method of fabricating a capacitor, comprising:

forming a container in an insulating layer overlying a semiconductor substrate;

lining the container with a hemispherical grained silicon layer;

depositing a titanium nitride layer over the hemispherical grained silicon layer;

and

recessing the hemispherical grained silicon layer to a depth of between about 100 Å to about 500 Å below a top of the container by exposing the hemispherical grained silicon layer to a tetramethyl ammoniumhydroxide solution comprising between about 1 and about 4 weight percent tetramethyl ammoniumhydroxide at a temperature between about  $40^\circ\text{C}$  and about  $65^\circ\text{C}$ .

41. (Original) The method of Claim 40, wherein the tetramethyl ammoniumhydroxide solution comprises about 2.25 weight percent tetramethyl ammoniumhydroxide.

42. (Original) The method of Claim 40, wherein the temperature is about 40°C.

43. (Original) The method of Claim 40, further comprising recessing the titanium nitride layer before recessing the hemispherical grained silicon layer.

44. (Original) The method of Claim 43, wherein recessing the titanium nitride layer comprises exposing the titanium nitride layer to an etchant chosen from the group consisting of an ammonium hydroxide/peroxide mixture (APM) and a hydrochloric acid/peroxide mixture (HPM).

45. (Previously presented) The method of Claim 44, wherein the recessing the titanium nitride layer comprises employing an APM with between about 0.33 and about 4.8 weight percent  $H_2O_2$  and between about 0.18 and about 3.9 weight percent  $NH_4OH$ .

46. (Original) The method of Claim 44, wherein the hydrochloric acid peroxide mixture comprises between about 0.33 and about 4.8 weight percent  $H_2O_2$  and between about 0.18 and about 4.9 weight percent HCl.

47. (Original) The method of Claim 40, wherein forming the container comprises anisotropically etching the insulating layer through a mask.

48. (Original) The method of Claim 40, wherein lining the container with a hemispherical grained silicon layer comprises a process from the group consisting of a low pressure CVD, a silicon deposition followed by a vacuum anneal, and a gas phase nucleation process.

49. (Original) A cell capacitor in a DRAM chip, comprising:

a structural layer overlying a semiconductor substrate, the structural layer having a container, the container having a wall, the wall having a top terminus;

a bottom electrode extending vertically along the wall,

wherein the bottom electrode comprises a metal nitride layer and a hemispherical grained silicon layer, wherein a top surface of the bottom electrode is about 100 Å to about 500 Å below the top terminus.

50. (Original) The cell capacitor of Claim 49, wherein the metal nitride layer comprises titanium nitride.

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51. (Original) The cell capacitor of Claim 49, wherein the structural layer is an insulating layer.

52. (Original) The cell capacitor of Claim 51, wherein the insulating layer is an oxide layer.

53. (Original) The cell capacitor of Claim 52, wherein the oxide layer comprises borophosphosilicate glass.

54-61. (Cancelled).